1. A process for wafer scale packaging, comprising:

providing a semiconductor wafer, including chip images separated by a kerf area and having a topmost passivating layer through which pass connecting studs;

forming a polymeric body having a plurality of metal posts in contact with, and fixed to, said connecting studs and passing vertically through said polymeric body from said studs; and

wherein said posts are of a diameter and height and of a material that they can bend to absorb stress due to thermal mismatch between said semiconductor wafer and said polymeric body.

2. The process of claim 1 wherein said polymeric body is a polyimide or a silicone elastomer or benzocyclobutene.

3. The process of claim 1 further comprising forming via holes in said polymeric body and then forming the conducting posts inside the via holes.

4. The process of claim 3 wherein said via holes are formed by chemical etching or by laser drilling.

5. The process of claim 3 wherein said metal posts of formed by electroplating or by electroless plating.

6. The process of claim 1 wherein a bending force exerted at a free end of a metal post of length L displaced by an amount d, is according to a formula $F = (3YId)/L^3$, where Y = Young's modulus and I = moment of inertia.

7. The process of claim 1 wherein said polymeric body is laid down by spin coating or by dipping or by spraying or in the form of a dry film with an adhesive undercoating.

8. A process for wafer scale packaging, comprising the sequential steps of:

(a) providing a semiconductor wafer, including chip images separated by a kerf area and having a topmost passivating layer through which pass connecting studs;

(b) depositing a planarizing layer of polyimide over the passivating layer and then patterning and etching said polyimide layer to form openings over the connecting studs;

(c) depositing a UBM layer on said polyimide layer, depositing a first layer of photoresist on the UBM layer, and then patterning the photoresist to leave uncovered areas of the UBM layer that define a common distribution network comprising chip-level redistribution networks connected to each other in the kerf;

(d) by means of electroplating, depositing a first layer of metal on all areas of the UBM layer not covered by photoresist;

(e) removing the first layer of photoresist and selectively removing all parts of the UBM layer that are not covered by said first layer of metal;

(f) laying down a layer of polymeric material and forming therein via holes that extend down to the level of the common distribution network;

(g) by means of electroplating, depositing a second layer of metal on all metallic areas not covered by the second layer of polymeric material until the via holes have been overfilled with said second metal layer, thereby forming posts with projections that extend by an amount above the layer of polymeric material;

(h) by means of electroplating, forming solder bumps centered around and attached to, said post projections; and

(i) slicing the wafer into individual chips, thereby cutting all lines in the kerf area and electrically dividing said common distribution network into chip-level redistribution networks.

9. The process of claim 8 wherein said polymeric body is a polyimide or a silicone elastomer or benzocyclobutene.

10. The process of claim 8 wherein said polymeric body is a layer having a thickness of between about 20 and 250 microns.

11. The process of claim 8 wherein the step of forming via holes in the layer of polymeric material further comprises using a photo sensitive version of the polyimeric material which is exposed through a mask and then developed to form the holes.

12. The process of claim 8 wherein the step of forming via holes in the layer of polymeric material further comprises using a photoresist mask in conjunction with a hard mask over the polymeric material and then etching the polymeric material.

13. The process of claim 8 wherein the step of forming via holes in the layer of polymeric material further comprises using laser drilling.

14. The process of claim 8 wherein said second metal layer has a thickness between about 20 and 250 microns and is selected from the group of consisting of copper, gold, solder, and aluminum .

15. The process of claim 11 wherein said photosensitive version provides a negative image of the mask which causes the via holes to be wider closest to the second layer of metal.

16. The process of claim 11 further comprising:

using a photosensitive version of the polymeric material that provides a positive image of the mask and that has upper and lower surfaces;

employing an imaging system that has a low depth of focus; and

focusing in a plane midway between said surfaces, thereby causing said via holes to be narrowest at a point halfway down the holes.

17. The process of claim 8 further comprising etching back the layer of polymeric material to generate a lollipop structure from the post and solder bump combination.

18. The process of claim 8 further comprising coating the uncovered portions of the

posts with a UBM layer before forming the solder bumps.

19. A process for wafer scale packaging, comprising the sequential steps of:

(a) providing a semiconductor wafer containing integrated circuits, including a topmost passivating layer through which pass conductive studs that connect to points within said integrated circuits;

(b) laying down a layer of polymeric material and forming therein via holes that overlie and extend down to said conductive studs;

(c) by means of electroless plating, depositing a layer of metal on all metallic areas not covered by polymeric material until the via holes have been overfilled with said metal layer thereby forming posts with projections that extend above the layer of polymeric material by an amount;

(d) by means of electroless plating, forming solder bumps centered around and attached to, said post projections; and

(e) slicing the wafer into individual chips.

20. The process of claim 19 wherein said polymeric body is a polyimide or a silicone elastomer or benzocyclobutene.

21. The process of claim 19 wherein said polyimeric body is a layer having a thickness of between about 20 and 250 microns.

22. The process of claim 19 wherein the step of forming via holes in the layer of polymeric material further comprises using a photosensitive version of the polymeric material which is exposed through a mask and then developed to form the holes.

23. The process of claim 19 wherein the step of forming via holes in the layer of polymeric material further comprises using a photoresist mask, together with a hard mask, over the polymeric material and then etching the polymeric material.

24. The process of claim 19 wherein the step of forming via holes in the layer of polymeric material further comprises using laser drilling.

25. The process of claim 22 wherein said photosensitive version provides a negative image of the mask which causes the via holes to be wider closest to the second layer of metal.

26. The process of claim 22 further comprising:

using a photosensitive version of the polymeric material that provides a positive image of the mask and that has upper and lower surfaces;

employing an imaging system that has a low depth of focus; and

focusing in a plane midway between said surfaces, thereby causing said via holes to be narrowest at a point halfway down the holes.

27. The process of claim 19 wherein the amount that the posts project above the layer of polyimeric material is between about 10 and 75 microns.

28. The process of claim 19 further comprising coating the uncovered portions of the posts with a UBM layer before forming the solder bumps.

29. The process of claim 19 wherein, in step (d) instead of electroless plating, the solder bumps are laid down using screen printing or stenciling.

30. A process for wafer scale packaging, comprising the sequential steps of:

(a) providing a semiconductor wafer containing an integrated circuit, including a topmost passivating layer through which pass conductive studs that connect to points within said integrated circuits;

(b) depositing a contacting layer of metal over the passivating layer;

(c) laying down a layer of photoresist and forming therein via holes that extend down to the contacting metal layer;

(d) by means of electroplating, depositing a layer of metal on all contacting metal areas not covered by photoresist until the via holes have been filled with said metal layer;

(e) removing the layer of photoresist, thereby forming freestanding metal posts;

(f) without attacking said posts, removing the contacting metal layer;

(g) spreading over the entire wafer a layer of polymeric material whereby part of the posts remain uncovered;

(h) forming solder bumps centered around and attached to, said post projections; and

(i) slicing the wafer into individual chips.

31. A wafer scale package, comprising:

a semiconductor wafer, including chip images separated by a kerf area and having a topmost passivating layer through which pass connecting studs;

a polymeric body having a plurality of metal posts in contact with, and fixed to, said connecting studs and passing vertically through said polymeric body from said studs; and

wherein said posts are of a diameter and height and of a material that they can bend to absorb stress due to thermal mismatch between said semiconductor wafer and said polymeric body.

32. The package of claim 31 wherein said polymeric body is a polyimide or a silicone elastomer or benzocyclobutene.

33. The package of claim 31 wherein said polymeric body has a thickness between about 20 and 250 microns.

34. The process of claim 31 wherein said metal posts have a width between about 10 and 200 microns.

35. The process of claim 31 wherein said metal posts are plated copper.

36. The package of claim 31 wherein a bending force exerted at a free end of a metal post of length L, displaced by an amount d, is according to a formula $F = (3YId)/L^3$, where Y = Young's modulus and I = moment of inertia.